ABSTRACT

A system and method for early evaluation in micropipeline processors to improve performance is provided. The present invention presents a design methodology where a micropipeline processor block (*e.g.,* a binary full adder) is capable of computing a result based on the arrival of only a subset of inputs. In general, early evaluation allows micropipeline processor blocks to operate in parallel, where they might otherwise operate sequentially because of data arrival dependencies; thereby improving performance of the micropipeline processors.

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